

**Government of Karnataka**  
**Department of Technical Education**  
**Board of Technical Examinations, Bengaluru**

Course Title: <b>Industrial Automation Lab</b>	Course Code : <b>15EC64P</b>
Semester : <b>6</b>	Course Group : <b>Core</b>
Teaching Scheme in Hrs (L:T:P) : <b>0:2:4</b>	Credits : <b>3</b>
Type of course : <b>Tutorial + Practical</b>	Total Contact Hours : <b>78</b>
CIE : <b>25 Marks</b>	SEE : <b>50 Marks</b>

### Prerequisites

Knowledge of electronic devices and logic systems

### Course Objectives

1. Compare the semiconductor devices with power electronics devices.
2. Applications of power control devices
3. Design and simulate PLC circuits

### Course Outcomes

*On completion of the course student should able to.*

1. Design and analyse the working of MOSFET, IGBT, SCR controlled rectifier circuits using R-C triggering circuit.
2. Demonstrate the functionality of Thyristor circuits such as light dimmer circuit, UJT relaxation oscillator, and voltage commutated chopper.
3. Illustrate the speed control of motors and sequential timer using IC 555.
4. Understand and analyse Ladder diagram concept to test digital logic gates, Boolean expression, Demorgan's theorem.
5. Illustrate the Ladder program for DOL starter, Stair case light, Water level controller, Conveyer control, and Lift control applications.
6. Analyse and implement any Simple industrial electronics circuit, PLC programming.

Course Outcome		CL	Linked Experiments	Linke d PO	Teachin g Hrs
CO1	Design and analyze the working of MOSFET, IGBT, SCR controlled rectifier circuits using R-C triggering circuit.	<i>R/U/A</i>	Unit-1: Part-A: E:1 to 2	1,2,3,4, 10	12
CO2	Demonstrate the functionality of Thyristor circuits such as light dimmer circuit, UJT relaxation oscillator, and voltage commutated chopper.	<i>U/A</i>	Unit-1: Part-A: E:3 to 5	1,2,3,4, 10	09
CO3	Illustrate the speed control of motors and sequential timer using IC 555.	<i>U/A</i>	Unit-1:Part A: E:6 to 9	1,2,3,4, 10	12
CO4	Understand and analyze Ladder diagram concept to test digital logic gates, Boolean expression, Demorgan's theorem	<i>R/U/A</i>	Unit-1: Part B: E:10 to 12	1,2,3,4, 10	12
CO5	Illustrate the Ladder program for DOL	<i>U/A/E</i>	Unit-1: Part B:	1,2,3,4,	21

	starter, Stair case light, Water level controller, Conveyer control, and Lift control applications.		E:13 to 18	10	
<b>CO6</b>	Analyze and implement any Simple industrial electronics circuit using PLC programming	<i>U/A/E/C</i>	Unit-2	1,2,3,4,5,8,9,10	06 (off-class)
<b>Two CIE/IA Tests</b>					<b>06</b>
<b>Total sessions</b>					<b>78</b>

**Legend:**R-Remember, U-Understand, A-Application, E-Evaluate, C-Create, CL-Cognitive Level, and PO-Program Outcome

## Mapping Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes									
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
CO1	*	*	*	*	--	--	--	--	--	*
CO2	*	*	*	*	--	--	--	--	--	*
CO3	*	*	*	*	--	--	--	--	--	*
CO4	*	*	*	*	--	--	--	--	--	*
CO5	*	*	*	*	--	--	--	--	--	*
CO6	*	*	*	*	*	--	--	*	*	*

## Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
<b>Industrial Automation Lab</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>3</b>	<b>1</b>	--	--	<b>1</b>	<b>1</b>	<b>3</b>

**Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.**

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.  
 If  $\geq 40\%$  of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3  
 If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2  
 If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1  
 If  $< 5\%$  of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

## Course Contents

### Unit-1: Tutorials and Graded Exercises

**72 Hours**

Sl. No.	Topic/Exercises	Duration (Hr)
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<b>Part-A: Power electronics devices experiments</b>		
1	Determination of holding current and break-over voltage of an SCR.	3
2	Full-wave controlled rectifier circuit using R-C triggering circuit	3
3	Light dimmer circuit using DIAC and TRIAC.	3
4	SCR triggering by UJT relaxation oscillator (Using Kit)	3
5	Voltage commutated chopper both constant frequency & variable frequency. (Using Kit)	3
6	Single phase to single phase cycloconverter (Using Kit)	3
7	Speed control of Universal motor. (Using Kit)	3
8	Speed control of stepper motor using inverter in clockwise & anti-clockwise direction. (Using Kit)	3
9	Sequential timer using IC 555.	3
10	Servicing/Maintenance of UPS (Only study experiments)	6

<b>Part-B: PLC Programming experiments</b>		
10	Study of PLC kit, practicing of basic programs.	3
11	Write the ladder diagram to test digital logic gates ( two, three and four inputs)	6
12	Write the ladder diagram for three variable Boolean expressions and test the output. Example: $Y = (\overline{A+B+C}) + (BC)$ and $Z = (\overline{A+B+C}) + (\overline{B+C})$ .	3
13	Write the ladder diagram to verify Demorgan's theorem.	3
14	Write the ladder diagram for DOL starter and test the output	3
15	Writing the ladder diagram and execute the Stair case light application	3
16	Writing the ladder diagram and execute the Water level controller application	3
17	Writing the ladder diagram and execute the Conveyer control application	3
18	Writing the ladder diagram and execute the Lift control application.	6
<b>Two Internal Assessment Tests(CIE)</b>		6
<b>Total</b>		<b>72</b>

**Unit 2: Student Activities [CIE- 05 Marks]**

**6 Hours**

Sl. No.	Activity	Duration (Hrs)
1	Visit and study the applications of Thyristors used in any nearby electrical power station.	06
2	Design the simple industrial electronics circuit/application by using any power semiconductor devices such as Thyristors, power diode, BJT, MOSFET etc.	
<b>Execution Mode</b>		
1. At least 4 students per batch. Every batch is assigned any one of the activities. 2. Assessment shall be made based on quality of activity, presentation/demonstration and report as per rubrics.		

### Institutional Activity (No marks)

The following are suggested institutional activities, to be carried out at least one activity during the semester. The course teacher/coordinator is expected to maintain the relevant record (Containing, Activity name, Resource persons and their details, duration, venue, student feedback, etc) pertaining to Institutional activities.

Sl. No.	Activity
1	Organize hands-on practice on design and implementation of Power electronic circuits, PLC and SCADA.
2	Organize a seminar/Guest lecture on Industrial applications of Thyristors.

### References

1. Overview of Industrial Process Automation - KLS Sharma, Elsevier Publication
2. Power Electronics handbook, 3rd edition-Muhammad H. Rashid- Elsevier, ISBN: 978-0-12-382036-5
3. Programmable Logic Controllers- John W.Webb and Ronald A Reis (Principle and applications)(Fifth Edition).
4. Programmable Logic Controllers -Programming Methods and Applications, John R. Hackworth and Frederick D. Hackworth, Jr.
5. <http://www.engineersgarage.com/articles/plc-programmable-logic-controller>
6. [https://en.wikipedia.org/wiki/Programmable\\_logic\\_controller](https://en.wikipedia.org/wiki/Programmable_logic_controller)
7. <https://www.circuitlogix.com>
8. [www.electronicprojects.org/](http://www.electronicprojects.org/)
9. <http://www.asic-world.com/>
10. <http://www.electronics-tutorials>
11. <http://www.circuitstoday.com>
12. <http://www.allaboutcircuits.com>
13. [http://onlinemas.weebly.com/uploads/6/3/9/4/6394050/lab\\_manual\\_shafeeq.pdf](http://onlinemas.weebly.com/uploads/6/3/9/4/6394050/lab_manual_shafeeq.pdf)
14. <http://ezhil-ecesait.webs.com/Power-Electronics-Lab-Manual.pdf>

### Course Delivery

The course will be delivered through two-hour tutorials and four-hour hands-on practice per week. Tutorial shall be imparted before the conduction of the experiment. Student activities are off-class and presentation/report evaluation is during assigned lab sessions.

## Course Assessment and Evaluation Scheme

### Master Scheme

Assessment Method	What		To Whom	Assessment mode /Frequency /timing	Max. Marks	Evidence Collected	Course Outcomes
Direct assessment	CIE	IA	Students	Two tests <sup>+</sup>	10	Blue Books	1 to 6
				Record <sup>@</sup>	10	Record Book	1 to 6
				Activity <sup>*</sup>	05	Report/Sheets	1 to 6
	SEE	End exam		End of the course	50	Answer Scripts at BTE	1 to 6
	Total			75			
Indirect assessment	Student feedback on course		Students	Middle of the Course	Nil	Feedback Forms	1 to 3 Delivery of course
	End of course survey			End of the Course	Nil	Questionnaires	1 to 6 Effectiveness of delivery instructions & assessment methods

**Legends:** CIE-Continuous Internal Evaluation, SEE- Semester End-exam Evaluation

<sup>+</sup> Every I.A. test shall be conducted as per SEE scheme of valuation. However, scored marks shall be scaled down to 10. Average of two tests, by rounding off any fractional part thereof to next higher integer, shall be considered for CIE/ IA.

<sup>\*</sup>Students should do activity as per the list of suggested activities/ similar activities with prior approval of the teacher. Activity process must be initiated well in advance so that it can be completed well before the end of the term.

<sup>@</sup>Record Writing: average of marks allotted for all experiments shall be considered; fractional part of the average shall be rounded-off to next higher integer.

### Composition of CLs

Sl. No.	Cognitive Levels (CL)	Weightage (%)
1	Remembering	20
2	Understanding	30
3	Applying	40
4	Evaluate	05
5	Create	05
<b>Total</b>		<b>100</b>

### Continuous Internal Evaluation (CIE) pattern

#### (i) Student Activity (5 marks)

The student activities in Unit-2 or similar activities can be assigned

**(ii) Model of rubrics for assessing student activity (for every student)**

Dimension	Scale					Marks (Example)
	1 Unsatisfactor y	2 Developing	3 Satisfactory	4 Good	5 Exemplary	
1. Information search and Collection.	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3
2. Full-fills team roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2
3. Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5
4. Listening Skills	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3
<b>Total marks</b>						ceil(13/4)= 4

**(iii) CIE/IA Tests (10 Marks)**

Two tests have to be conducted in accordance SEE pattern and the marks shall be scaled down to 10. Average of two tests, rounding-off any fractional part to next higher integer, shall be considered for CIE/IA.

**(iv) Record Evaluation (10 Marks)**

Every experiment shall be assigned marks for a scale of 10 after its conduction based on student's performance and quality of write-up. Average of them, by rounding-off any fractional part to next higher integer, shall be considered for CIE/IA.

**Semester End-exam Evaluation (SEE) Scheme**

Sl. No.	Scheme	Max. Marks
1	<b>Part-A:</b> Writing circuit diagram of one experiment with Procedure /Tabular column/ Nature of graph/waveform, formula for calculations.	10
2	<b>Part-B:</b> Writing Ladder diagram and program of one experiment with procedure.	10
3	Conduction of Part-A experiment and result.	10
4	Execution of part-B experiment and result.	15
5	Viva-voce	05
<b>TOTAL</b>		<b>50</b>
<b>Note:</b>		
1. Candidate is expected to submit the Lab record for the examination		
2. Student shall not be allowed to conduct directly if he/she is unable to write at least one correct circuit diagram.		

## Laboratory Resource Requirements

Equipments and kits Requirement: For a batch of 20 students

Sl. No.	Equipment	Quantity
1	Industrial electronics Trainer kits	05 each
2	PLC Trainer Kit with the following modules: 1. DOL starter 2. Stair case light application. 3. Water level controller application 4. Conveyer control application 5. Lift control application.	05 each
3	Patch cards( different lengths)	100
4	Dual trace oscilloscope.	05
5	Digital multimeters	05
6	Tachometers	05

## Model Questions for Practice and Semester End Examination

**Note:** The questions in the question bank are indicative but not exhaustive.

### Part-A

1. Determine holding current and break-over voltage of a given SCR experimentally.
2. Construct Light dimmer circuit using DIAC and TRIAC and verify the result.
3. Demonstrate Full wave controlled rectifier circuit using RC-triggering circuit.
4. Design Voltage commutated chopper both constant frequency & variable frequency.
5. Design the circuit of SCR triggered by UJT relaxation oscillator.
6. Verify the output for Single phase to single phase cycloconverter circuit .
7. Construct and verify the output for Speed control of Universal motor.
8. Construct and verify the output for Speed control of stepper motor using inverter in clockwise & anti-clockwise direction.
9. Construct the Sequential timer using IC-555 and verify the output.

### Part-B

10. Write the ladder diagram to test digital logic gates (two, three and four inputs).
11. Write the ladder diagram for three variable Boolean expressions and test the output.  
Example:  $Y = (\bar{A} + B + C) + (BC)$  and  $Z = (\bar{A}B + C) + (B + C)$ .
12. Write the ladder diagram to verify Demorgan's theorem.
13. Write the Ladder diagram for DOL starter and test the output.
14. Write the ladder diagram and execute the Stair case light application.
15. Write the ladder diagram and execute the Water level controller application.
16. Write the ladder diagram and execute the Conveyer control application.
17. Write the ladder diagram and execute the Lift control application.

**End**