Government of Karnataka

Department of Technical Education
Board of Technical Examinations, Bengaluru

Course Title: **PCB Design and Fabrication Lab**		Course Code	: **15EC56P**
Semester	: **5**	Credits	: **3 Credits**
Teaching Scheme in Hrs (L:T:P)	: **0:2:4**	Course Group	: **Core**
Type of course	: **Tutorial + Practical**	Total Contact Hours	: **78**
CIE	: **25 Marks**	SEE	: **50 Marks**

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Prerequisite

Knowledge of analog and digital circuits.

Course Objectives

1. Understand the need for PCB Design and steps involved in PCB Design and Fabrication process.
2. Familiarize Schematic and layout design flow using Electronic Design Automation (EDA) Tools.

Course Outcomes

At the end of the course, the students will be able to attain the following COs

Course Outcome		CL	Experiments linked	Linked PO	Teaching Hrs
CO1	Appreciate the necessity and evolution of PCB, types and classes of PCB.	***R/U/A***	Unit-1 Chapter 1	1,2,4,10	03
CO2	Understand the steps involved in schematic, layout, fabrication and assembly process of PCB design.	***R/U/A***	Unit-1 Chapter 2 and practice exercises.	1,2,3,4,10	12
CO3	Understand basic concepts of transmission line, crosstalk and thermal issues	***R/U/A***	Unit-1 Chapter 4	1,2,3,4,5, 10	03
CO4	Design (schematic and layout) PCB for analog circuits, digital circuits and mixed circuits.	***R/U/A /AN/E V/C***	Unit 2: Part A Exercises1 to 11	1,2,3,4,5, 10	45
CO5	Design (schematic and layout) and fabricate PCB for simple circuits.	***R/U/A /AN/E V/C***	Unit 2: Part B, Unit 3	1,2,3,4,5, 10	06
				Two CIE/IA Tests	06
				Project Activity	03
				Total Sessions	**78**

Legend: E- Experiment, R-Remember, U-Understand, A-Application, AN-Analyze ,EV-Evaluate, C-Create, CL-Cognitive Level, PO-Program Outcome

Note: Total sessions include two tests

Mapping Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes									
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
CO1	*	*	*	--	--	--	--	--	--	*
CO2	*	*	*	*	--	--	--	--	--	*
CO3	*	*	*	*	*	--	--	--	--	*
CO4	*	*	*	*	*	--	--	--	--	*
CO5	*	*	*	*	*	--	--	--	--	*

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
PCB Design and Fabrication Lab	3	3	3	3	3	--	--	--	--	3

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.
If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3
If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2
If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1
If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Contents

Unit-1: Tutorials and Practice Exercises 12Hours

Tutorial		
Sl. No.	**Topic/Exercises**	**Duration (Hr.)**
1	**Introduction to PCB** • Definition and Need/Relevance of PCB • Background and History of PCB • Types of PCB • Classes of PCB Design • Terminology in PCB Design • Different Electronic design automation (EDA) tools and comparison.	03

2	**PCB Design Process** • PCB Design Flow, Placement and routing • Steps involved in layout design • Artwork generation Methods - manual and CAD • General design factor for digital and analog circuits • Layout and Artwork making for Single-side, double-side and Multi-layer Boards. • Design for manufacturability • Design-specification standards	03
3	**Introduction to PCB Fabrication & Assembly** • Steps involved in fabrication of PCB. • PCB Fabrication techniques-single, double sided and multilayer • Etching: chemical principles and mechanisms • Post operations- stripping, black oxide coating and solder masking • PCB component assembly processes	03
4	**Transmission lines and crosstalk** • **Transmission Line:** Transmission lines and its effects Significance of Transmission line in Board design Types of Transmission lines. • **Crosstalk:** The crosstalk in transmission lines Crosstalk control in PCB design parts, planes, tracks, connectors, terminations Minimization of crosstalk. • **Thermal issues:** Thermal mapping of design	03
	Total Duration (Hr.)	**12**

	Practice Exercises	**09Hrs**
2	**Using any Electronic design automation (EDA) software, Practice following PCB Design steps (Open source EDA Tool KiCad Preferable)** **Example circuit:** Basic RC Circuit • Schematic Design: Familiarization of the Schematic Editor, Schematic creation, Annotation, Netlist generation • Layout Design: Familiarization of Footprint Editor, Mapping of components, Creation of PCB layout Schematic • Create new schematic components • Create new component footprints	

Unit – 2: Graded Exercises 45 Hours

Part-A: Design PCB (schematic and Layout) for following exercises.		
Sl.	**Graded Exercises**	**Duration**

No.		(Hr.)
1	Regulator circuit using 7805.	3
2	Inverting Amplifier or Summing Amplifier using op-amp	3
3	Full-wave Rectifier	3
4	Astable or Monostable multivibrator using IC555	3
5	RC Phase-shift or Wein-bridge Oscillator using transistor.	3
6	Full-Adder using half-adders.	3
7	4 bit binary /MOD N counter using D-Flip flops.	3
8	One open-ended (analog/ digital/mixed circuit) experiments of similar nature and magnitude of the above are to be assigned by the teacher (Student is expected to solve and execute/simulate independently).	3
9-11	Design a 8051 Development board having • **Power section** consisting of IC7805, capacitor, resistor, headers, LED • **Serial communication section** consisting of MAX 232, Capacitors, DB9 connector, Jumper, LEDs • **Reset & Input/ output sections** consisting of89C51 Microcontroller, Electrolytic Capacitor, Resistor, Jumper, Crystal Oscillator, Capacitors Note: For SEE any one section among three shall be considered as one exercise.	9
Part-B: Fabricate single-side PCB for simple network		
Sl. No.	**Graded Exercises**	**Duration (Hr.)**
1	Fabricate single-sided PCB, mount the components and assemble in a cabinet for any one of the circuits mentioned in Part-A of graded exercises.	6
	Two Internal Assessment Tests	6
	Total Duration (Hr.)	**45**

Tools and materials required for PCB fabrication:

1. Open source EDA Tool KiCad.
2. Single-sided copper clad sheet.
3. Diluted Acidic solution for copper etching purpose with plastic tray.
4. Tapes and pads for layout design of different dimensions.
5. Hand drilling/Power drilling machine.
6. Tool kit (tong, hand gloves etc.)

Unit – 3: Project/Student Activities [CIE- 05 Marks]

***Note*:The following activities or similar activities for assessing CIE (IA) for 5 marks (Any one)**

Sl. No.	Activity	Duration (Hrs)

1	Design and fabricate PCB for any one project, mount the components and assemble in a cabinet: Some of the projects are listed below which is just a guideline for selecting the project. Students can also select any other project with the advice of his teacher. List of sample circuit: 1. Touch plate switches – transistorized or 555 based 2. Doorbell/cordless bell 3. Clapping switch and IR switch 4. Blinkers 5. Cell charger, battery charger, mobile charger 6. Fire/smoke/intruder alarm 7. Liquid level controller 8. Counters 9. Audio amplifiers	**03**

Execution Mode

1. Every student should perform Project activity independently as assigned by the teacher based on interest of the student. Student can also choose any other similar activity with a prior approval from the concerned teacher.
2. Project activities shall be carried out throughout the semester and present the project report at the end of the semester.
3. Report-size shall be qualitative and not to exceed 6 pages;
4. Each of the activity can be carried out off-class; however, demonstration/presentation should be done during laboratory sessions.
5. Assessment shall be made based on quality of activity, presentation/demonstration and report.
6. Assessment is made based on quality of work as prescribed by the following rubrics table.

Institutional Activity (No marks)

The following are suggested institutional activities, to be carried out at least one during the semester. The course teacher/coordinator is expected to maintain the relevant record (Containing, Activity name, Resource persons and their details, duration, venue, student feedback, etc) pertaining to Institutional activities

Sl. No.	Activity
1	Organize seminar on free-open source EDA software
2	Conduct quiz on PCB Design fundamentals.

References

1. Printed Circuit Board by RS Khandpur, Tata McGraw Hill Education Pvt Ltd., New Delhi
2. Electronic Product Design Volume-I by S D Mehta, S Chand Publications
3. Open source EDA Tool KiCad Tutorial: http://kicad-pcb.org/help/tutorials/
4. PCB Fabrication user guide page: http://www.wikihow.com/Create-Printed-Circuit-Boards , http://www.siongboon.com/projects/2005-09-07_home_pcb_fabrication/ , http://reprap.org/wiki/MakePCBInstructions#Making_PCBs_yourself

5. PCB Fabrication at home(video): https://www.youtube.com/watch?v=mv7Y0A9YeUc, https://www.youtube.com/watch?v=imQTCW1yWkg

Course Delivery

The idea behind this course delivery is to provide relevant tutorial and hands-on practice concurrently. The course will be normally delivered through two-hour tutorials and four-hour hands-on practice per week; hands-on practice shall include practice exercises and graded exercises. Normally, one-hour tutorial followed by two-hour hands-on practice is recommended in each class. In Unit-1, tutorials and practice may be carried out concurrently. However, graded exercise (Unit-II) can also be covered at appropriate point of tutorials of Unit-1. Activities are carried-out off class.

Course Assessment and Evaluation Scheme

Master Scheme

Assessment Method	What		To Whom	Assessment mode /Frequency /timing	Max. Marks	Evidence Collected	Course Outcomes
Direct assessment	CIE	IA	Students	Two tests+	**10**	Blue Books	1 to 5
				Record@	**10**	Record Book	1 to 5
				Activity*	**05**	Report/Sheets	1 to 5
	SEE	End exam		End of the course	**50**	Answer Scripts at BTE	1 to 5
				Total	**75**		
Indirect assessment	Student feedback on course		Students	Middle of the Course	Nil	Feedback Forms	1 to 2 & Delivery of course
	End of course survey			End of the Course	Nil	Questionnaires	1 to 5, Effectiveness of delivery instructions & assessment methods

Legends: CIE-Continuous Internal Evaluation, SEE- Semester End-exam Evaluation

1. I.A. test shall be conducted as per SEE scheme of valuation. However obtained marks shall be reduced to 10 marks. Average marks of two tests shall be rounded off to the next higher digit.
2. Rubrics to be devised appropriately by the concerned faculty to assess Student activities.

***S**tudents should do activity as per the list of suggested activities/ similar activities with prior approval of the teacher. Activity process must be initiated well in advance so that it can be completed well before the end of the term.

@Record Writing: Average of marks allotted for each experiment; fractional part of average shall be rounded-off to next higher integer.

Composition of CLs

Sl. No.	Cognitive Levels (CL)	Weightage (%)
1	Remembering	10
2	Understanding	20
3	Applying	30
4	Analyze	15
5	Evaluate	15
6	Create	10
	Total	**100**

Continuous Internal Evaluation (CIE) pattern

(i) Student Activity (5 marks): The student activities in Unit-3 or similar activities can be assigned by the teacher

Execution Notes:

1. Each student assigned at least one activity listed in Unit-3 based on interest of the students. Student can also choose any other similar /relevant activity with prior approval from the concerned teacher.
2. Teacher is expected to observe and record the progress of students' activities
3. Assessment is made based on quality of work as prescribed by the following **rubrics** table

(ii) Model of rubrics for assessing student activity (for every student)

Dimension	Scale					Marks (Example)
	1 Unsatisfactory	2 Developing	3 Satisfactory	4 Good	5 Exemplary	
1. Research and gathering information	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3
2. Full-fills team roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2
3. Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5
4. Listen to other team mates	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3
					Total marks	ceil(13/4)= 4

(iii) CIE/IA Tests (10 Marks)

Two tests shall be conducted in accordance with SEE pattern and the marks shall be scaled down to 10. Average of two tests, rounding-off any fractional part thereof to next higher integer, shall be considered for CIE/IA.

(iv) Record Evaluation (10 Marks)

Every experiment shall be given marks, in the scale of 10, after its conduction based on student's performance and quality of write-up. Average of them, by rounding-off any fractional part thereof to next higher integer, shall be considered for CIE/IA.

Semester end-exam evaluation (SEE) Scheme

Sl. No.	Scheme	Max. Marks
1	Short questions onUnit-1 (only write-up)	05
2	Design PCB (schematic and layout) for any given circuit (similar complexity as in graded exercises) Schematic Design-10 Marks Layout Design-15 Marks Fabrication–10 Marks Component mounting & soldering-5Marks	40
5	Viva-voce	05
TOTAL		**50**

Note:

1. Candidate shall submit lab-record for the examination.
2. Student shall be allowed to design even if she/he is unable to write the procedure/steps.
3. Candidate must be given the relevant circuit diagram.

Model Questions for Practice and Semester End Examination

Graded Exercises

Design and Fabricate PCB for the given circuit in the following list. Also, mount and solder the components.

1. Full-wave bridge Rectifier.
2. Astable or mono-stable multivibrator using IC555
3. RC Phase shift Oscillator using transistor
4. BJT Amplifier in Common Emitter Configuration
5. Full Adder using half adder.
6. 4-bit binary or MOD N counter using D Flip-flop or JK flip-flop.
7. 4-bit shift-register using JK Flip-flop in any one of PIPO/SIPO/PISO/SISO modes.
8. 89C51/8051 Development board Serial communication section consist of MAX 232, Capacitors, DB9 connector, Jumper, LEDs
9. PCB for-89C51/8051 Development board Reset & Input/ output sections consist of 89C51 Microcontroller, Electrolytic Capacitor, Resistor, Jumper, Crystal Oscillator, Capacitors
10. Regulated power supply (Only filter and regulation sections).
11. Sinosoidal Oscillator using Op-amp.
12. Sinosoidal Oscillator using BJT.
13. Sinosoidal Oscillator using JFET.
14. Active filter circuit using Op-amp

End

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